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10/772,945	02/04/2004	Peter J. Fricke	200310842-1	5316

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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
3404 E. Harmony Road
Mail Stop 35
FORT COLLINS, CO 80528

EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
09/21/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

JERRY.SHORMA@HP.COM
ipa.mail@hp.com
jessica.l.fusek@hp.com

Office Action Summary	Application No.	Applicant(s)	
	10/772,945	FRICKE ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-33 and 36-59* is/are pending in the application.

4a) Of the above claim(s) *2,12-15,17-25,36,37,42-46 and 50-54* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8-11,16,26-33,38-41,47-49 and 55-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

In view of the IDS filed on 07/09/2009, PROSECUTION IS HEREBY REOPENED. A new rejection based on DiMaria et al. (this reference was submitted by applicant in an IDS filed on 07/09/2009) is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Lynne A. Gurley/

Supervisory Patent Examiner, Art Unit 2811

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 4-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitation of "a tunnel junction layer", as recited in dependent claim 5, is unclear as to the structural relationship between the tunnel junction layer and the memory array.

The claimed limitation of "a tunnel junction layer thickness of about 3-5 nanometers", as recited in dependent claim 5, is unclear as to which claimed element has the thickness of about 3-5 nanometers.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-6, 8-11,16, 26-33, 38-41, 47-49 and 55-59, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over DiMaria et al. ("Dense Alpha

Particle-Immune Memory Device", IBM Tech Disclosure Bulletin, Vol. 23, No. 1, June 1980, pp 381-382) in view of Lee et al. (6,881,994) and Rinerson et al. (6,834,008), **or in the alternative**, over Lee et al. (6,881,994) in view of DiMaria et al. ("Dense Alpha Particle-Immune Memory Device", IBM Tech Disclosure Bulletin, Vol. 23, No. 1, June 1980, pp 381-382).

DiMaria et al. teach in figure 1 and related text a memory device comprising:

a memory cell disposed at each cross point of a first conductor and a second conductor, each memory cell having exactly two terminals and having a storage element FG and a control element coupled in series between a first conductor Al1 and a second conductor Al2, each control element including a tunnel junction SiO_2 and a silicon-rich oxide insulator INJECTOR, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected.

DiMaria et al. do not teach using the memory device as a memory array device, wherein the memory array comprising a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points.

Lee et al. teach in figure 34 and related text using a memory device as a memory array device, wherein the memory array comprising a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points (see e.g. figure 52), wherein a memory cell disposed at each cross point, each memory cell having exactly two terminals and having a

storage element and a control element coupled in series between a row conductor and a column conductor.

Rinerson et al. teach in figures 1-3 and related text using a memory device as a memory array device, wherein the memory array comprising a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, wherein a memory cell disposed at each cross point, each memory cell having exactly two terminals.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the memory cell of DiMaria et al. as a memory array device, wherein the memory array comprising a multiplicity of row conductors and a multiplicity of column conductors, and wherein the row conductors and column conductors being arranged to cross at cross-points, in order to use the device in a practical memory device application which is well known in the art to be formed as a memory array device.

The combination is motivated by the teachings of Rinerson et al. who point out the advantages of using cross point architecture.

Note that a memory array structure inherently comprises a multiplicity of row conductors and a multiplicity of column conductors, wherein the row conductors and column conductors being arranged to cross at cross-points.

In the alternative:

Lee et al. teach in figure 34 and related text a memory array comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points (see e.g. figure 52), and

b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor, each control element including a tunnel junction and a silicon oxide insulator.

Lee et al. do not teach a control element including a tunnel junction and a silicon-rich oxide insulator, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected.

DiMaria et al. teach in figure 1 and related text a memory device comprising a memory cell disposed at each cross point of a first conductor and a second conductor, each memory cell having exactly two terminals and having a storage element FG and a control element coupled in series between a first conductor Al1 and a second conductor Al2, each control element including a tunnel junction SiO_2 and a silicon-rich oxide insulator INJECTOR, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a control element including a tunnel junction and a silicon-rich oxide insulator, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected in Lee et al.'s device in order to improve the device characteristics by enhancing the electric field of the structure.

The combination is motivated by the teachings of DiMaria et al. who point out the advantages of using a control element including a tunnel junction and a silicon-rich oxide insulator.

Note further that it is well known in the art to use silicon rich dielectric injectors in the control element of a memory device.

Regarding claims 5-6 and 8-10, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a control element of each memory cell comprises a tunnel junction layer thickness of about 3-5 nanometers, and the storage element of each memory cell comprises an anti-fuse, a fuse, a tunnel junction, a state-change layer and a chalcogenide, in prior art's device in order to use known memory control and storage elements, of which official notice is taken.

Regarding claims 4 and 11, the silicon-rich insulator of each memory cell of prior art's device is electrically isolated from the silicon-rich insulators of all other memory cells, and includes a row conductors are arranged in mutually orthogonal relationship with the column conductors.

Regarding claim 16, prior art's device includes a memory cell disposed at each cross-point, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for controlling being

coupled in series between a row conductor and a column conductor, and each means for controlling including a silicon-rich insulator.

Regarding claim 26, prior art's device includes a tunnel-junction layer SiN over the silicon rich insulator and a second conductive layer over the tunnel-junction layer. Prior art does not state that the memory cell is formed by a method of

b) depositing and patterning a first conductive layer over the substrate, and

c) forming and patterning a second conductive layer,

However, these process limitations would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 38, prior art's device includes a first interlayer dielectric over the storage layer and having an opening through the first interlayer dielectric and extending to the storage layer, and having a conductive material therein as a middle electrode, this conductive layer is contiguous with the storage layer.

Prior art does not state that the memory cell is formed by a method of

b) depositing and patterning a first conductive layer over the substrate, and

c) forming and patterning a second conductive layer,

d) forming and patterning first and second interlayer dielectrics over the storage layer,

e) forming an opening through the first interlayer dielectric and extending to the storage layer,

g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode.

However, these process limitations would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Regarding claims 30, 47 and 55, prior art's device includes a second interlayer dielectric is formed over the storage layer, forming vias as required though the second interlayer dielectric to selectively interconnect memory cells of the memory arrays.

Prior art does not state that the memory cell is formed by a method of

b) depositing and patterning a first conductive layer over the substrate, and

c) forming and patterning a second conductive layer,

d) forming and patterning first and second interlayer dielectrics over the storage layer,

e) forming an opening through the first interlayer dielectric and extending to the storage layer,

g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode.

k) forming vias as required though the second interlayer dielectric, and repeating steps b) through k) until a desired number of memory array layers have been formed.

However, these process limitations would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Regarding claims 27-29, 31-33, 39-41, 48-49 and 56-57, prior art's device includes a memory array comprising a multiplicity of the memory cells, a substrate carrying electronics and an IC comprising a multilayer memory, wherein a multiplicity of the memory arrays are arranged in memory layers.

Regarding claims 58-59, prior art's device includes two terminals of the two terminal memory cell disposed at each cross-point comprise the row conductor and column conductor respectively.

Claims 1, 3-6, 8-11,16, 26-33, 38-41, 47-49 and 55-59, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (6,881,994) in view of Bhattacharyya (7,012,297), Wolf et al. (4,717,943) and Bass Jr. et al. (4,870,470), **or in the alternative**, over Bass Jr. et al. in view of Lee et al. (6,881,994) and Rinerson et al. (6,834,008).

Lee et al. teach in figure 34 and related text a memory array comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points (see e.g. figure 52), and

b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor, each control element including a tunnel junction and a silicon oxide insulator.

Lee et al. do not teach a control element including a tunnel junction and a silicon-rich oxide insulator, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected.

Bhattacharyya teach in figure 11 and related text a control element including a tunnel junction and a silicon-rich oxide insulator 1154, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected.

Wolf et al. teach in figure 2 and related text a control element including a tunnel junction 16 and a silicon-rich oxide insulator 20, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected.

Bass Jr. et al. teach in figure 6 and related text a control element including a tunnel junction and a silicon-rich oxide insulator 35, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a control element including a silicon-rich oxide insulator, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected in Lee et al.'s device in order to improve the device characteristics by enhancing the electric field of the structure.

The combination is motivated by the teachings of Bhattacharyya who points out the advantages of using a silicon-rich oxide insulator.

Note further that it is well known in the art to use silicon rich dielectric injectors in the control element of a memory device.

In the alternative:

Bass Jr. et al. teach in figure 6 and related text a memory array (see e.g. abstract) comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points (inherent in an array structure), and

b) a memory cell disposed therein, each memory cell having two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor, each control element including a tunnel junction and a silicon-rich

oxide insulator 30 or 35, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected.

Bass Jr. et al. do not teach using the memory structure as a memory cell disposed at each cross-point, wherein each memory cell having exactly two terminals.

Lee et al. teach in figure 34 and related text a memory cell disposed at each cross-point, wherein each memory cell having exactly two terminals.

Rinerson et al. teach in figures 1-3 and related text a memory cell 115, 215, 315 disposed at each cross-point, wherein each memory cell having exactly two terminals.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the memory cell at each cross-point, wherein each memory cell having exactly two terminals in Lee et al.'s device in order to improve the device characteristics by using cross point architecture.

The combination is motivated by the teachings of Rinerson et al. who point out the advantages of using cross point architecture.

Regarding claims 5-6 and 8-10, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a control element of each memory cell comprises a tunnel junction layer thickness of about 3-5 nanometers, and the storage element of each memory cell comprises an anti-fuse, a fuse, a tunnel junction, a state-change layer and a chalcogenide, in prior art's device in order to use known memory control and storage elements, of which official notice is taken.

Regarding claims 4 and 11, the silicon-rich insulator of each memory cell of prior art's device is electrically isolated from the silicon-rich insulators of all other memory cells, and includes a row conductors are arranged in mutually orthogonal relationship with the column conductors.

Regarding claim 16, prior art's device includes a memory cell disposed at each cross-point, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for controlling being coupled in series between a row conductor and a column conductor, and each means for controlling including a silicon-rich insulator.

Regarding claim 26, prior art's device includes a tunnel-junction layer SiN over the silicon rich insulator and a second conductive layer over the tunnel-junction layer.

Prior art does not state that the memory cell is formed by a method of

b) depositing and patterning a first conductive layer over the substrate, and

c) forming and patterning a second conductive layer,

However, these process limitations would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the

patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 38, prior art's device includes a first interlayer dielectric over the storage layer and having an opening through the first interlayer dielectric and extending to the storage layer, and having a conductive material therein as a middle electrode, this conductive layer is contiguous with the storage layer.

Prior art does not state that the memory cell is formed by a method of

b) depositing and patterning a first conductive layer over the substrate, and

c) forming and patterning a second conductive layer,

d) forming and patterning first and second interlayer dielectrics over the storage layer,

e) forming an opening through the first interlayer dielectric and extending to the storage layer,

g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode.

However, these process limitations would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Regarding claims 30, 47 and 55, prior art's device includes a second interlayer dielectric is formed over the storage layer, forming vias as required though the second interlayer dielectric to selectively interconnect memory cells of the memory arrays.

Prior art does not state that the memory cell is formed by a method of

b) depositing and patterning a first conductive layer over the substrate, and

c) forming and patterning a second conductive layer,

d) forming and patterning first and second interlayer dielectrics over the storage layer,

e) forming an opening through the first interlayer dielectric and extending to the storage layer,

g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode.

k) forming vias as required though the second interlayer dielectric, and repeating steps b) through k) until a desired number of memory array layers have been formed.

However, these process limitations would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Regarding claims 27-29, 31-33, 39-41, 48-49 and 56-57, prior art's device includes a memory array comprising a multiplicity of the memory cells, a substrate carrying electronics and an IC comprising a multilayer memory, wherein a multiplicity of the memory arrays are arranged in memory layers.

Regarding claims 58-59, prior art's device includes two terminals of the two terminal memory cell disposed at each cross-point comprise the row conductor and column conductor respectively.

Response to Arguments

Applicant argues that the notice of non-compliant appeal brief dated May 8, 2009, is erroneous and should be withdrawn.

The examiner agrees with applicant's argument, and the notice of non-compliant appeal is hereby withdrawn.

Applicant argues that Lee, Bhattacharyya, Wolf, and Bass, do not include the claimed subject matter, "particularly the claimed memory cell comprising a control element with a tunnel junction and a silicon-rich insulator that injects current into the tunnel junction when the memory cell is selected", because Bhattacharyya Wolf, and Bass, "do not explicitly describe how data is read from the memory cell it teaches", and since the gate stack of Bhattacharyya, Wolf, and Bass do not control write and read operations of its associated memory cell, then the gate stack cannot read on the control element recited in claim 1.

Bhattacharyya, Wolf, and Bass are merely cited to teach an artisan that a control element can include a tunnel junction and a silicon-rich oxide insulator. Said control element is suggested to modify Lee et al.'s device such that Lee et al.'s device includes

a control element comprising a tunnel junction and a silicon-rich oxide insulator, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected.

Conclusion

Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 07/09/2009 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

O.N.
9/18/2009

/ORI NADAV/
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800